Docket No.

244824US2

### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Tamio IKEHASHI, et al.

SERIAL NO: New Application

GAU:

FILED:

Herewith

**EXAMINER:** 

FOR:

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

### **INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97**

COMMISSIONER FOR PATENTS ALEXANDRIA, VIRGINIA 22313

SIR

Applicant(s) wish to disclose the following information.

#### REFERENCES

- The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

### **RELATED CASES**

- Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

#### CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- □ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

### **DEPOSIT ACCOUNT**

Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number <u>15-0030</u>. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Tamio IKEHASHI, et al.

SERIAL NO: New Application

FILED: HEREWITH

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

# **STATEMENT OF RELEVANCY**

# Reference AO (2002-246571) on Form PTO-1449:

A structure of a dynamic memory cell having a gate underneath the floating body. An impact ionization is used to write data "1".

### Reference AP (2003-31693) on Form PTO-1449:

A structure of a dynamic memory cell having an n+ layer underneath the buried oxide.

### Reference AQ(5-347419) on Form PTO-1449:

A memory structure that uses a bipolar transistor to write data. Unlike our memory cell, the bipolar transistor is isolated from the floating gate (1110) that stores memory data (Figs. 26, 36, 37).

| Form PTO 1449 U.S. DEPARTMENT OF COMMERCE (Modified) PATENT AND TRADEMARK OFFICE  LIST OF REFERENCES CITED BY APPLICANT                      |  |                                   |          | ATTY DOCKET NO.<br>244824US2  |                 | SERIAL NO.  New Appliction |                                       |
|--|--|-----------------------------------|----------|-------------------------------|-----------------|----------------------------|---------------------------------------|
|  |  |                                   |          | APPLICANT                     |                 |                            |                                       |
|  |  |                                   |          | Tamio IKEHASHI, et al.        |                 |                            |                                       |
|  |  |                                   |          | FILING DATE                   |                 | GROUP                      |                                       |
|  |  |                                   |          | Herewith                      |                 |                            |                                       |
| U.S. PATENT DOCUMENTS  |  |                                   |          |                               |                 |                            |                                       |
| EXAMINER   |  | DOCUMENT                          |          |                               | Γ               | SUB                        | FILING DATE                           |
| INITIAL  |  | NUMBER                            | DATE     | NAME                          | CLASS           | CLASS                      | IF APPROPRIATE                        |
|  | AA   | 5,355,330                         | 10/11/94 | Dai HISAMOTO, et al.          | ļ <u>.</u>      | _                          |                                       |
|  | AB   |                                   |          |                               | ļ               |                            |                                       |
|  | AC   |                                   |          |                               | <u> </u>        |                            |                                       |
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|  | AL   |                                   |          |                               |                 |                            |                                       |
|  | AM   |                                   |          |                               |                 |                            |                                       |
|  | AN   |                                   |          |                               |                 |                            |                                       |
| FOREIGN PATENT DOCUMENTS   |  |                                   |          |                               |                 |                            |                                       |
|  |  | DOCUMENT<br>NUMBER                | DATE     | COUNTRY                       |                 | TRANSLATION YES NO         |                                       |
|  | AO   | 2002-246571                       | 08/30/02 | Japan (with English Abstract) |                 |                            | X                                     |
|  | AP   | 2003-31693                        | 01/31/03 | Japan (with English Abstract) |                 |                            | Х                                     |
|  | AQ   | 5-347419                          | 12/27/93 | Japan (with English Abstract) |                 |                            | X                                     |
|  | AR   |                                   | •        |                               | •               |                            |                                       |
|  | AS   | -                                 |          |                               |                 |                            |                                       |
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|  | AV   |                                   |          |                               | •               |                            | · · · · · · · · · · · · · · · · · · · |
| OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)  |  |                                   |          |                               |                 |                            |                                       |
|  | T. Ohsawa, et al., "Memory Design Using One Transistor Gain Cell on SOI", ISSCC DIGEST OF TECHNICAL PAPERS, ISSCC 2002/ SESSION 9/ DRAM AND FERROELECTRIC MEMORIES/9.1, Feb. 2002, pgs 152-153 and 454 |                                   |          |                               |                 |                            |                                       |
|  | AX   |                                   |          |                               |                 |                            |                                       |
|  | AY   |                                   |          |                               |                 |                            |                                       |
|  | AZ   | Additional References sheet(s) at |          |                               |                 |                            | erences sheet(s) attached             |
| Examiner   |  |                                   |          |                               | Date Considered |                            |                                       |
| *Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in |  |                                   |          |                               |                 |                            |                                       |
| conformance and not considered. Include copy of this form with next communication to applicant.  |  |                                   |          |                               |                 |                            |                                       |